ATTACHMENT A: SEARCH HISTORY

L Number	Hits	Search Text	DB	Time stamp
34	16841	semiconductor and memory and cell and array and (sense adj amplifier\$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/06/28 10:51
35	5615	(semiconductor and memory and cell and array and (sense adj amplifier\$1)) and (control with (generat\$3 with circuit))	IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/06/28 11:08
36	2679	((semiconductor and memory and cell and array and (sense adj amplifier\$1)) and (control with (generat\$3 with circuit))) and (first with signal) and (second with	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/06/28
37	1728	signal) and (third with signal) (((semiconductor and memory and cell and array and (sense adj amplifier\$1)) and (control with (generat\$3 with circuit))) and (first with signal) and (second with signal) and (third with signal)) and (first with (terminal or node)) and (second with (terminal or node))	IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/28 11:09
38	280	<pre>((((semiconductor and memory and cell and array and (sense adj amplifier\$1)) and (control with (generat\$3 with circuit))) and (first with signal) and (second with signal) and (third with signal)) and (first with (terminal or node)) and (second with (terminal or node))) and (first with switch) and (second with switch) and (third with switch)</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/28
39	176	(((((semiconductor and memory and cell and array and (sense adj amplifier\$1)) and (control with (generat\$3 with circuit))) and (first with signal) and (second with signal) and (third with signal)) and (first with (terminal or node)) and (second with (terminal or node))) and (first with switch) and (second with switch) and (third with switch)) and (power with supply) and ground	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/28
40	94	((((((semiconductor and memory and cell and array and (sense adj amplifier\$1)) and (control with (generat\$3 with circuit))) and (first with signal) and (second with signal) and (third with signal)) and (first with (terminal or node)) and (second with (terminal or node)) and (first with switch) and (second with switch) and (second with switch) and (third with switch)) and (power with supply) and ground) and (fourth with switch)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/28
41	2	(((((((semiconductor and memory and cell and array and (sense adj amplifier\$1)) and (control with (generat\$3 with circuit))) and (first with signal) and (second with signal) and (third with signal)) and (first with (terminal or node)) and (second with (terminal or node))) and (first with switch) and (second with switch) and (second with switch) and (third with switch)) and (power with supply) and ground) and (fourth with switch)) and (first with recycl\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/28 11:11

				0004/05/55
42	1	<pre>(((((((semiconductor and memory and cell and array and (sense adj amplifier\$1)) and (control with (generat\$3 with circuit))) and (first with signal) and</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/06/28 11:12
		(second with signal) and (third with signal)) and (first with (terminal or node)) and (second with (terminal or node))) and (first with switch) and	IBM_TDB	
		(second with switch) and (third with switch)) and (power with supply) and ground) and (fourth with switch)) and		
43	94	<pre>(second with recycl\$3) ((((((semiconductor and memory and cell and array and (sense adj amplifier\$1)) and (control with (generat\$3 with</pre>	USPAT; US-PGPUB; EPO; JPO;	2004/06/28 11:12
		circuit))) and (first with signal) and (second with signal) and (third with signal)) and (first with (terminal or node)) and (second with (terminal or node))) and (first with switch) and	DERWENT; IBM_TDB	
		node))) and (first with switch) and (second with switch) and (third with switch)) and (power with supply) and ground) and (fourth with switch)) and (control with signal)		
44	80	<pre>((((((((((((((((((((((((((((((((((((</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/06/28 11:12
•		(second with signal) and (third with signal)) and (first with (terminal or node)) and (second with (terminal or node))) and (first with switch) and (second with switch) and (third with switch)) and (power with supply) and ground) and (fourth with switch)) and (control with signal)) and (first with control)	IBM_TDB	
45	71	<pre>((((((((((semiconductor and memory and cell and array and (sense adj amplifier\$1)) and (control with (generat\$3 with circuit))) and (first with signal) and (second with signal) and (third with signal)) and (first with (terminal or node)) and (second with (terminal or node))) and (first with switch) and (second with switch) and (third with switch)) and (power with supply) and ground) and (fourth with</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/28 11:12
46		switch)) and (control with signal)) and (first with control)) and (second with control) and (third with control)	IICDAM.	2004/06/29
40	53	<pre>(((((((((((semiconductor and memory and cell and array and (sense adj amplifier\$1)) and (control with (generat\$3 with circuit))) and (first with signal) and (second with signal) and (third with signal)) and (first with (terminal or node)) and (second with (terminal or node))) and (first with switch) and (second with switch) and (third with switch)) and (power with supply) and ground) and (fourth with switch)) and (control with signal)) and</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/28
		(first with control)) and (second with control) and (third with control)) and 365/\$7.ccls.		

				0001100100
47	5	(((((((((semiconductor and memory and	USPAT;	2004/06/28
		cell and array and (sense adj	US-PGPUB;	11:14
		amplifier\$1)) and (control with	EPO; JPO;	
		(generat\$3 with circuit))) and (first	DERWENT;	
	1	with signal) and (second with signal) and	IBM_TDB	
		(third with signal)) and (first with		
	1	(terminal or node)) and (second with		
		(terminal or node))) and (first with		
		switch) and (second with switch) and		
		(third with switch)) and (power with		
		supply) and ground) and (fourth with		
		switch)) and (control with signal)) and		
		(first with control)) and (second with		
		control) and (third with control)) and		
		365/\$7.ccls.) and 365/207.ccls.		
48	37	(((((((((semiconductor and memory and	USPAT;	2004/06/28
		cell and array and (sense adj	US-PGPUB;	11:14
		amplifier\$1)) and (control with	EPO; JPO;	
		(generat\$3 with circuit))) and (first	DERWENT;	
		with signal) and (second with signal) and	IBM_TDB	
	[(third with signal)) and (first with	_	
		(terminal or node)) and (second with		
		(terminal or node))) and (first with		
		switch) and (second with switch) and		
		(third with switch)) and (power with		
		supply) and ground) and (fourth with		
1		switch)) and (control with signal)) and		
		(first with control)) and (second with		
		control) and (third with control)) and		
		365/\$7.ccls.) and (reduc\$3 with power)		